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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2115	20

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,540	GARRITSEN ET AL.	
	Examiner	Art Unit	
	Pranav Chandrasekhar	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-3,10,11,13 and 15 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Atkinson [US Pat No. 6,691,236].

2. As per claim 1, Atkinson teaches

receiving a change indication related to a system power supply [col. 11 lines 53-60.];

adjusting a first clock [col. 11 lines 63-65]; and

adjusting a controller power supply voltage [col. 11 lines 63-65].

3. As per claim 15, Atkinson teaches

detecting a change in a system power supply [col. 11 lines 53-60];

notifying the graphics controller of the change [col. 11 lines 53-60];

receiving an indication of power reduction in the graphics controller [col. 11 lines 53-60]; and

providing a set of available clock frequencies to the graphics controller [col. 9 lines 29-32; col. 9 lines 46-52].

4. As per claim 2, Atkinson further teaches signaling a BIOS with an indication of a change related to the system power supply [col. 4 lines 50-58].

5. As per claim 3, Atkinson further teaches

receiving a set of one or more available clock rates[col. 9 lines 46-52];

checking a state of the graphics controller [col. 9 lines 58-61];

choosing a desired clock rate from the set of available clock rates [col. 9 lines 46-52];

adjusting a second clock to conform to the desired clock rate [col.9 lines 46-52. The VCLK is viewed as a second clock]; and wherein:

adjusting the first clock comprises reducing a rate of the first clock [col. 10 lines 11-19. The MCLK is viewed as a first clock.]; and

adjusting the controller power supply voltage comprises reducing the controller power supply voltage [col. 10 lines 20-27].

6. As per claim 10, Atkinson further teaches

adjusting the first clock comprises increasing a rate of the first clock [col. 10 line 45. The memory clock (first clock) is viewed as being at a lower rate prior to being set to its maximum rate.]; and

adjusting the controller power supply voltage comprises increasing the controller power supply voltage [col. 10 line 36].

7. As per claim 11, Atkinson further teaches increasing a clock rate of a second clock [col. 10 lines 55-60. The VCLK is viewed as being a second clock.]

8. As per claim 13, Atkinson further teaches detecting a change related to a system power supply [col. 11 lines 53-60.];

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 20-22 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson [US Pat No. 6,691,236] in view of Suboh [US Pat No. 5,524,249].

10. As per claim 36, Atkinson teaches

receiving a change indication related to a system power supply [col. 11 lines 53-60];

reducing a rate of a first clock [col. 10 lines 11-19];

signaling a BIOS with an indication of a change related to the system power supply [col. 4 lines 50-58];

receiving a set of one or more available clock rates [col. 9 lines 46-52];

checking a state of a graphics controller [col. 9 lines 58-61];

choosing a desired clock rate from the set of available clock rates [col. 9 lines 46-52]; and

adjusting a second clock to conform to the desired clock rate [col. 9 lines 46-52].

Atkinson does not explicitly teach disabling a first portion of circuitry responsive to checking the state of the graphics controller.

Suboh teaches disabling a first portion of circuitry responsive to checking the state of the graphics controller [col. 4 lines 20-32; col. 4 lines 46-48. The PCLK is viewed as a first portion of the circuitry.].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Atkinson and Suboh to disable a first portion of circuitry in response to a state of reduced power of a graphics controller in order to conserve power that may be consumed by an enabled portion of circuitry.

11. As per claim 20, Atkinson does not explicitly teach disabling a first portion of circuitry of the graphics controller.

Suboh teaches disabling a first portion of circuitry of the graphics controller [col. 4 lines 20-32; col. 4 lines 46-48. The PCLK is viewed as a first portion of the circuitry].

12. As per claim 21, Atkinson does not explicitly teach disabling the first portion of circuitry responsive to checking the state of the graphics controller.

Suboh further teaches disabling a first portion of the circuitry responsive to checking the state of the graphics controller [col. 4 lines 20-32; col. 4 lines 46-48]

13. As per claim 22, Atkinson does not explicitly teach enabling the first portion of the graphics controller.

Suboh further teaches enabling the first portion of the graphics controller [col. 8 lines 24-27].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Atkinson and Suboh to enable a first portion of a graphics controller in order to facilitate power consumption at a regular or increased level.

14. Claims 4,5,8,9,14 and 23-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson [US Pat No. 6,691,236].

15. As per claim 4, Atkinson does not explicitly teach disabling a CLUT.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Atkinson to disable a CLUT in order to conserve power.

16. As per claim 5, Atkinson does not explicitly teach disabling a CLUT responsive to checking the state of the graphics controller.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Atkinson disable the CLUT responsive to checking the state of the graphics controller since the disabling of the CLUT must be triggered by a power conserving state of the graphics controller.

17. As per claim 9, Atkinson further teaches

a controller power supply voltage associated with a controller power supply external to the graphics controller [Fig 1].

Atkinson does not explicitly teach adjusting the controller power supply including programming the controller power supply with a signal.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Atkinson to program a controller power supply with a signal in order to facilitate the change of supply voltage to the controller.

18. As per claim 23, Atkinson teaches

a power supply input configured to receive power at one of two available voltages [col. 10 lines 25-28];

a power supply control output [col. 10 lines 25-28];

a first clock [col. 9 lines 12-17]; and

a system power supply change input [col. 11 lines 53-60].

Atkinson does not explicitly teach the power supply input being configured to receive power at range of voltages.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Atkinson to facilitate the selection of a voltage from a range of voltages in order to provided intermediary levels of supply voltage as opposed to two specific voltage levels.

19. As per claim 24, Atkinson further teaches a first clock control output [col. 10 lines 11-19].

20. As per claim 25, Atkinson further teaches a memory coupled to the first clock [col. 7 lines 43-46].

21. As per claim 26, Atkinson further teaches

a second clock [col. 9 lines 46-52]; and

a second clock control output [col. 9 lines 46-52].

22. As per claim 27, Atkinson further teaches a memory coupled to the first clock [col. 7 lines 43-46].

23. As per claim 28, Atkinson does not explicitly teach the memory being integrated with other portions of the graphics controller on a single substrate.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Atkinson to integrate the memory with other portions of the graphics controller.

24. As per claim 29, Atkinson does not explicitly teach a voltage regulator coupled to the power supply input and the power supply control output.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Atkinson to incorporate a voltage regulator coupled to the power supply input and power supply control output in order to regulate the supply voltage to a desired voltage level depending on the operational mode of the graphics controller.

25. As per claim 8, Atkinson does not explicitly teach the controller power supply being associated with a controller power supply internal to the graphics controller.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Atkinson to incorporate a controller power supply internal to the graphics controller.

26. As per claim 14, Atkinson does not explicitly teach installing a software routine in a system containing the graphics controller, the software routine suitable for detecting the change related to the system power supply.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Atkinson to incorporate a software routine in a system containing the graphics controller to detect a change related to the system power supply.

27. As per claim 18, Atkinson and Powell do not explicitly teach

receiving a software routine for notifying the graphics controller; and wherein:

notifying the graphics controller comprises executing the software routine.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Atkinson and Powell to incorporate a software routine for notifying a graphics controller.

28. As per claim 19, Atkinson further teaches

programming the set of available clock frequencies [col. 9 lines 46-52];

29. As per claim 30, Atkinson does not explicitly teach the voltage regulator being integrated with other portions of the graphics controller on a single substrate.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Atkinson to integrate a voltage regulator with other portions of the graphics controller on a single substrate in order to facilitate the regulation of supply voltage to the controller to a desired value depending on the operational mode of the controller.

30. As per claim 31, Atkinson does not explicitly teach a VGA BIOS.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Atkinson to incorporate a VGA BIOS since the VGA BIOS must set the operational mode of the graphics controller.

31. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson [US Pat No. 6,691,236] in view of Chen [US Pat No. 6,489,953].

32. As per claim 12, Atkinson does not explicitly teach enabling a CLUT.

Chen teaches enabling a CLUT [col. 3 lines 16-20. The CLUT is viewed as being enabled].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Atkinson and Chen to incorporate a CLUT to facilitate functions relating to color in the graphics controller.

33. Claims 6,7,16-19,32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson [US Pat No. 6,691,236] in view of Powell [US Pat No. 6,618,042].

34. As per claim 16, Atkinson does not teach receiving a signal from the graphics controller to reduce brightness of a display

Powell teaches receiving a signal from the graphics controller to reduce brightness of a display [col. 5 lines 17-24.The reduction in brightness of display is viewed as being the result of a signal received from the graphics controller.].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Atkinson and Powell to incorporate brightness reduction of display in order to conserve power.

35. As per claim 17, Atkinson does not teach reducing brightness of a display

Powell teaches reducing brightness of a display [col. 5 lines 17-24].

36. As per claim 6, Atkinson does not explicitly teach notifying a system to reduce brightness of display.

Powell teaches notifying a system to reduce brightness of display [col. 4 lines 1-8].

37. As per claim 7, Atkinson and Powell do not explicitly teach notifying a system including notifying a chipset directly.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Atkinson and Powell to notify a chipset directly in order to conserve power immediately after receiving a trigger for an operation mode of power reduction.

38. As per claim 32, Atkinson does explicitly teach brightness output being configured to signal to a system that a reduction in brightness of the display is appropriate.

Powell teaches brightness output being configured to signal to a system that a reduction in brightness of the display is appropriate [col. 4 lines 1-8].

39. As per claim 33, Atkinson and Powell do not explicitly teach the brightness output being suitable to couple directly to a video control chipset.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Atkinson and Powell to couple the brightness output directly to a video control chipset since it would be advantageous for the video control signals to directly effect the brightness level of the display.

40. As per claim 18, Atkinson and Powell do not explicitly teach

receiving a software routine for notifying the graphics controller; and wherein:

notifying the graphics controller comprises executing the software routine.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Atkinson and Powell to incorporate a software routine for notifying a graphics controller.

41. As per claim 19, Atkinson further teaches

programming the set of available clock frequencies [col. 9 lines 46-52];

42. Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson [US Pat No. 6,691,236] in view of Powell [US Pat No. 6,618,042] as applied to claim 32 above, and further in view of Chen [US Pat No. 6,489,953].

43. As per claim 34, Atkinson teaches

a system interface including the system power supply input [12 Fig 1. The pwer supply input is viewed as being contained in a system interface.];

a video interface including the second clock and the second clock control output [2 Fig 1. VCLK (second clock) and its control output are viewed as being contained in a video interface.];

a power control interface including the power supply input and the power supply control output [12 Fig 1; The power supply input and power supply control output are viewed as being contained in a power control interface.];

a memory control interface including the first clock [MCLK, 5 Fig 1. The MCLK (first clock) and memory are viewed as being contained in a memory control interface.]; and

a control unit coupled to the system interface, the video interface, the power control interface and the memory control interface [col. 11 lines 63-65; col. 11 lines 53-60; col. 9 lines 46-52; col. 10 lines 11-19. The changes brought about in the video interface and memory control interface due to changes in the system interface and power control interface are viewed as being executed by a control unit.];

Atkinson and Powell do not explicitly teach

a 2D engine;

a 3D engine;

a CLUT coupled to the 3D engine and the 2D engine

Chen teaches

a 2D engine[60 Fig 3];

a 3D engine [62 Fig 3];

a CLUT coupled to the 3D engine and the 2D engine [66 Fig 3; col. 3 lines 16-20];

It would have been obvious to one of ordinary skill in the art to combine the teachings of Atkinson, Powell and Chen to incorporate a 2D engine, 3D engine and a CLUT coupled to the 3D engine and 2D engine in order to facilitate enhanced graphics functions in the graphics controller.

44. As per claim 35, Atkinson teaches

a power supply input configured to receive power at one of two available supply voltages [12 Fig 1];

a power supply control output [VCC Fig 1];

a first clock [MCLK Fig 1];

a system power supply change input [col. 11 lines 53-60];

a first clock control output [col. 10 lines 11-19];

a second clock [VCLK Fig 1];

a second clock control output [col. 9 lines 46-52];

a system interface including the system power supply input [12 Fig 1. The power supply input is viewed as being contained in a system interface.];

a video interface including the second clock and the second clock control output [2 Fig 1. VCLK (second clock) and its control output are viewed as being contained in a video interface.];

a power control interface including the power supply input and the power supply control output [12 Fig 1; The power supply input and power supply control output are viewed as being contained in a power control interface.];

a memory control interface including the first clock [MCLK, 5 Fig 1. The MCLK (first clock) and memory are viewed as being contained in a memory control interface.]; and

a control unit coupled to the system interface, the video interface, the power control interface and the memory control interface [col. 11 lines 63-65; col. 11 lines 53-60; col. 9 lines 46-52; col. 10 lines 11-19. The changes brought about in the video interface and memory control interface due to changes in the system interface and power control interface are viewed as being executed by a control unit.].

Atkinson does not explicitly teach

a power supply input configured to receive power at a range of voltages;

a brightness output configured to signal to a system that a reduction in brightness of a display is appropriate;

a 2D engine;

a 3D engine;

a CLUT coupled to the 3D engine and coupled to the 2D engine;

Powell teaches

a brightness output configured to signal to a system that a reduction in brightness of a display is appropriate [col. 4 lines 1-8].

Powell does not teach

a power supply input configured to receive power at a range of voltages;

a 2D engine;

a 3D engine; and

a CLUT coupled to the 3D engine and coupled to the 2D engine;

Chen teaches

a 2D engine [60 Fig 3];

a 3D engine [62 Fig 3]; and

a CLUT coupled to the 3D engine and coupled to the 2D engine [66 Fig 3; COL. 3 lines 16-20];

Chen does not teach

a power supply input configured to receive power at a range of voltages;

It would have been obvious to combine the teachings of Atkinson, Powell and Chen to incorporate a 2D engine, 3D engine and CLUT coupled to the 3D engine and 2D engine in order to provide enhanced graphics functions to the graphics controller as well as providing power saving features in the form of brightness reduction of the display. Furthermore, it would have been obvious to one of ordinary skill in the art to configure the power supply input to receive power at a range of voltages as opposed to two fix voltages in order to utilize voltage levels associated with intermediary levels of power consumption.

Conclusion

45. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

46. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pranav Chandrasekhar whose telephone number is 703-305-8647. The examiner can normally be reached on 8:30 a.m.-5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 703-305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Pranav Chandrasekhar
June 7,2004

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